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REMARKS: Copy of amended paragraph no. 1 of U.S. Patent Application No. 10/632,215

Total Number of Pages (Including This One): 4

FROM: Jonathan M. Harris, Reg. No. 44,144, Direct Dial No. 713.238-8045

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ATTORNEY DOCKET NO. TI-35460 (1962-05417)

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[0001] This application claims priority to U.S. Provisional Application Serial No. 60/400,391 titled "JSM Protection," filed July 31, 2002, incorporated herein by reference.

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This application also claims priority to EPO Application No. 03291912.9, filed July 30, 2003 and entitled "Reformat Logic To Translate Between A Virtual Address And A Compressed Physical Address," incorporated herein by reference. This application also may contain subject matter that may relate to the following commonly assigned co-pending applications incorporated herein by reference: "System And Method To Automatically Stack And Unstack Java Local Variables," Serial No. **10/632,228**, filed July 31, 2003; "Memory Management Of Local Variables," Serial No. **10/632,067**, filed July 31, 2003; "Memory Management Of Local Variables Upon A Change Of Context," Serial No. **10/632,076**, filed July 31, 2003; "A Processor With A Split Stack," Serial No. **10/632,079**, filed July 31, 2003; "Using IMPDEP2 For System Commands Related To Java Accelerator Hardware," Serial No. **10/632,069**, filed July 31, 2003; "Test With Immediate And Skip Processor Instruction," Serial No. **10/632,214**, filed July 31, 2003; "Test And Skip Processor Instruction Having At Least One Register Operand," Serial No. **10/632,084**, filed July 31, 2003; "Synchronizing Stack Storage," Serial No. **10/631,422**, filed July 31, 2003; "Methods And Apparatuses For Managing Memory," Serial No. **10/631,252**, filed July 31, 2003; "Write Back Policy For Memory," Serial No. **10/631,185**, filed July 31, 2003; "Methods And Apparatuses For Managing Memory," Serial No. **10/631,205**, filed July 31, 2003; "Mixed Stack-Based RISC Processor," Serial No. **10/631,308**, filed July 31, 2003; "Processor That Accommodates Multiple Instruction Sets And Multiple Decode Modes," Serial No. **10/631,246**, filed July 31, 2003; "System To Dispatch Several Instructions On Available Hardware Resources," Serial No. **10/631,585**, filed July 31, 2003; "Micro-Sequence Execution In A Processor," Serial No. **10/632,216**, filed July 31, 2003; "Program Counter Adjustment Based On The Detection Of An Instruction Prefix," Serial No. **10/632,222**, filed July 31, 2003; "Synchronization Of Processor States," Serial No. **10/632,024**, filed July 31, 2003; "Conditional Garbage Based On Monitoring To Improve Real Time Performance," Serial No. **10/631,195**, filed July 31, 2003; "Inter-Processor Control," Serial No. **10/631,120**, filed July 31, 2003; "Cache Coherency In A Multi-Processor System," Serial No. **10/632,229**, filed July 31, 2003; "Concurrent Task Execution In A Multi-Processor, Single Operating System Environment," Serial No. **10/632,077**, filed July 31, 2003; and "A Multi-Processor Computing System Having A Java Stack Machine And A RISC-Based Processor," Serial No. **10/631,939**, filed July 31, 2003.

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**Please replace paragraph [0001] with the following amended paragraph:**

[0001] This application claims priority to U.S. Provisional Application Serial No. 60/400,391 titled "JSM Protection," filed July 31, 2002, incorporated herein by reference. This application also claims priority to EPO Application No. 03291912.9, filed July 30, 2003 and entitled "Reformat Logic To Translate Between A Virtual Address And A Compressed Physical Address," incorporated herein by reference. This application also may contain subject matter that may relate to the following commonly assigned co-pending applications incorporated herein by reference: "System And Method To Automatically Stack And Unstack Java Local Variables," Serial No. [[ ]]10/632,228, filed July 31, 2003, ~~Attorney Docket No. TI-35422 (1962-05401)~~; "Memory Management Of Local Variables," Serial No. [[ ]]10/632,067, filed July 31, 2003, ~~Attorney Docket No. TI-35423 (1962-05402)~~; "Memory Management Of Local Variables Upon A Change Of Context," Serial No. [[ ]]10/632,076, filed July 31, 2003, ~~Attorney Docket No. TI-35424 (1962-05403)~~; "A Processor With A Split Stack," Serial No. [[ ]]10/632,079, filed July 31, 2003, ~~Attorney Docket No. TI-35425 (1962-05404)~~; "Using IMPDEP2 For System Commands Related To Java Accelerator Hardware," Serial No. [[ ]]10/632,069, filed July 31, 2003, ~~Attorney Docket No. TI-35426 (1962-05405)~~; "Test With Immediate And Skip Processor Instruction," Serial No. [[ ]]10/632,214, filed July 31, 2003, ~~Attorney Docket No. TI-35427 (1962-05406)~~; "Test And Skip Processor Instruction Having At Least One Register Operand," Serial No. [[ ]]10/632,084, filed July 31, 2003, ~~Attorney Docket No. TI-35248 (1962-05407)~~; "Synchronizing Stack Storage," Serial No. [[ ]]10/631,422, filed July 31, 2003, ~~Attorney Docket No. TI-35429 (1962-05408)~~; "Methods And Apparatuses For Managing Memory," Serial No. [[ ]]10/631,252, filed July 31, 2003, ~~Attorney Docket No. TI-35430 (1962-05409)~~; "Write Back Policy For Memory," Serial No. [[ ]]10/631,185, filed July 31, 2003, ~~Attorney Docket No. TI-35431 (1962-05410)~~; "Methods And Apparatuses For Managing Memory," Serial No. [[ ]]10/631,205, filed July 31, 2003, ~~Attorney Docket No. TI-35432 (1962-05411)~~; "Mixed Stack-Based RISC Processor," Serial No. [[ ]]10/631,308, filed July 31, 2003, ~~Attorney Docket No. TI-35433 (1962-05412)~~; "Processor That Accommodates Multiple Instruction Sets And Multiple Decode Modes," Serial No.

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[[\_\_\_\_]]10/631,246, filed July 31, 2003, ~~Attorney Docket No. TI-35434 (1962-05413)~~; "System To Dispatch Several Instructions On Available Hardware Resources," Serial No. [[\_\_\_\_]]10/631,585, filed July 31, 2003, ~~Attorney Docket No. TI-35444 (1962-05414)~~; "Micro-Sequence Execution In A Processor," Serial No. [[\_\_\_\_]]10/632,216, filed July 31, 2003, ~~Attorney Docket No. TI-35445 (1962-05415)~~; "Program Counter Adjustment Based On The Detection Of An Instruction Prefix," Serial No. [[\_\_\_\_]]10/632,222, filed July 31, 2003, ~~Attorney Docket No. TI-35452 (1962-05416)~~; "Synchronization Of Processor States," Serial No. [[\_\_\_\_]]10/632,024, filed July 31, 2003, ~~Attorney Docket No. TI-35461 (1962-05418)~~; "Conditional Garbage Based On Monitoring To Improve Real Time Performance," Serial No. [[\_\_\_\_]]10/631,195, filed July 31, 2003, ~~Attorney Docket No. TI-35485 (1962-05419)~~; "Inter-Processor Control," Serial No. [[\_\_\_\_]]10/631,120, filed July 31, 2003, ~~Attorney Docket No. TI-35486 (1962-05420)~~; "Cache Coherency In A Multi-Processor System," Serial No. [[\_\_\_\_]]10/632,229, filed July 31, 2003, ~~Attorney Docket No. TI-35637 (1962-05421)~~; "Concurrent Task Execution In A Multi-Processor, Single Operating System Environment," Serial No. [[\_\_\_\_]]10/632,077, filed July 31, 2003, ~~Attorney Docket No. TI-35638 (1962-05422)~~; and "A Multi-Processor Computing System Having A Java Stack Machine And A RISC-Based Processor," Serial No. [[\_\_\_\_]]10/631,939, filed July 31, 2003, ~~Attorney Docket No. TI-35710 (1962-05423)~~.